Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

1. (Currently Amended) A method of providing an intermediate dielectric isolated silicon structure comprising the steps of:

forming a trench pattern on a semiconductor substrate;

forming a dielectric layer on the surfaces of said trench pattern;

forming a heavily doped buried p^+ layer around said trench pattern;

exposing semiconductor surface on the bottom of said trench pattern;

depositing silicon to fill said trench pattern;

forming buried porous silicon layer around said filled trench pattern;

oxidizing said buried porous silicon layer and forming a thin oxide over said deposited silicon surface; and

forming ~~said~~ isolated silicon islands from said deposited silicon.

2. (Currently Amended) The method of forming dielectric isolated silicon structure according to claim 1, wherein said ~~trench surface is lined with~~ dielectric layer is a silicon dioxide, formed using at least one of thermal oxidation, low pressure chemical vapor deposition (LPCVD) ~~and/or~~ and plasma enhanced CVD.

3. (Original) The method of forming dielectric isolated silicon structure according to claim 2, wherein said silicon dioxide liner thickness is approximately between 1000 °A and 2000 °A.

4. (Original) The method of forming dielectric isolated silicon structure according to claim 1, wherein said heavily doped buried p^+ layer is formed by implanting B^+ ions with a dose of approximately between 10^{15} and 10^{16} atom/cm^2.

5. (Original) The method of forming dielectric isolated silicon structure according to claim 4, wherein said buried p^+ layer depth is approximately between 4000 °A and 6000 °A.

6. (Original) The method of forming dielectric isolated silicon structure according to claim 1, wherein said silicon film filling the trench is selective epitaxial silicon.

7. (Currently Amended) The method of forming dielectric isolated silicon structure according to claim 6, wherein, said selective epitaxial film is deposited using methods of at least one of molecular beam epitaxy, low pressure CVD, plasma enhanced CVD, and ~~and/or~~ liquid phase epitaxy.

8. (Original) The method of forming dielectric isolated silicon structure according to claim 1, wherein said buried porous silicon layer is formed with anodic etching process comprising:

etching bath composition: 10% - 40% HF

current density: 10 - 60 mA/cm^2

9. (Currently Amended) The method of forming dielectric isolated silicon structure according to claim 1, wherein said buried porous silicon layer is oxidized at approximately between 850 and 1050 °C to form an isolating silicon layer.

10. (Currently Amended) The method of forming dielectric isolated silicon structure according to claim 9, wherein said isolating silicon dioxide layer ~~has~~ and said dielectric layer have a combined thickness of approximately between 4000 °A and 6000 °A.

11. (Currently Amended) The method of forming dielectric isolated silicon structure according to claim 1, wherein said forming isolated silicon islands comprises removing said ~~thermal~~ thin oxide ~~on epitaxial silicon layer is removed~~ to expose said silicon

islands[, with] using at least one of chemical mechanical polishing, wet, ~~and/or~~ and plasma etching methods.

12. (Currently Amended) A method of forming intermediate silicon dioxide isolated epitaxial silicon structure comprising the steps of:

forming a hard mask stack of silicon dioxide and silicon nitride on a single crystal silicon substrate;

forming a trench pattern in said single crystal silicon substrate;

forming a silicon dioxide layer on the surfaces of said trench pattern;

forming a heavily doped buried p^+ layer around said trench pattern;

reactive ion etching said silicon dioxide layer on said trench pattern surfaces to expose single crystal silicon at trench bottom, leaving oxide liner on the walls of said trench pattern;

depositing selective epitaxial silicon to fill said trench pattern;

removing said hard mask stack;

forming a resist pattern to fully mask said filled trench;

forming buried porous silicon layer around said filled trench;

oxidizing said buried porous silicon layer and forming a thin oxide over said epitaxial silicon surface; and

forming epitaxial silicon islands by removing said thin oxide layer from top of said epitaxial silicon surface, using at least one of ~~with~~ chemical mechanical polishing, wet etching methods, ~~and/or~~ and plasma etching methods.

13. (Original) The method of forming dielectric isolated silicon structure according to claim 12, wherein said silicon dioxide liner thickness is approximately between 1000 °A and 2000 °A.

14. (Original) The method of forming dielectric isolated silicon structure according to claim 12, wherein said heavily doped, buried p^+ layer is formed by implanting B^+ ions with a dose of approximately between 10^{15} and 10^{16} atom/cm^2.

15. (Original) The method of forming dielectric isolated silicon structure according to claim 14, wherein said buried p^+ layer depth is approximately between 4000 °A and 6000 °A.

16. (Original) The method of forming dielectric isolated silicon structure according to claim 12, wherein said buried porous silicon layer is formed with anodic etching process comprising:

etching bath composition: 10% - 40% HF

current density: 10 – 60 mA/cm^2

17. (Original) The method of forming dielectric isolated silicon structure according to claim 12, wherein said buried porous silicon layer is oxidized at approximately between 850 and 1050 °C.

18. (Original) The method of forming dielectric isolated silicon structure according to claim 17, wherein said isolating silicon dioxide layer has a thickness of approximately between 4000 °A and 6000 °A.

19. (Withdrawn) A silicon-dioxide isolated epitaxial silicon structure comprising:

epitaxial silicon filled trenches in silicon substrate and

isolated buried silicon dioxide layer surrounding said epitaxial silicon islands or regions.

20. (Withdrawn) The silicon-dioxide epitaxial silicon structure according to claim 19, wherein said isolating silicon dioxide layer has a thickness of approximately between 4000 and 6000 °A.